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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/680,158
Filing Date: October 08, 2003
Appellant(s): MOULI, CHANDRA

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GROUP 2800

Thomas J. D'Amico (Reg. No. 28,371)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/22/2006 appealing from the Office action mailed 5/24/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Ohsawa, T., et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE Journal of Solid-State Circuits, Vol. 37, No. 11 (Nov. 2002), p. 1510-22

6,838,322	Pham et al.	1-2005
6,313,486	Kencke et al.	11-2001
5,448,513	Hu et al.	9-1995
6,806,537	Matsumoto et al.	10-2004
5,307,305	Takasu	4-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 to 7, 11, 12, 17 to 21, 23, 24, 28 to 34, 37, 41 to 46, 47 to 53, 56, 57 and 62 to 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al. (IEEE 2002), Pham et a. (U.S. Patent No. 6,838,322) and Kencke et al. (U.S. Patent No. 6,313,486).

Ohsawa et al. show most aspects of the instant invention (e.g. Figures 1 to 3) including:

- ➢ an SOI substrate with two layer of opposite conductivity type (i.e. P and N)
- ➢ a partially depleted storage transistor located on said substrate's surface (e.g. Figures 1)

- first and second source/drain regions **n** with a body portion **p** there between
- a gate structure consisting of a gate electrode and insulating layer of silicon oxide
- a word line **WL** connected to said gate structure and a bit line **BL** connected to one of said source/drain regions

Ohsawa et al. do not show the storage transistor as a FinFET with the gate structure wrap around the body portion in at least two planes and consisting of a plurality of gates, the gate electrode comprising doped polysilicon or metal, the thickness of the insulating layer being thicker on the top of the body portion than on the sides, the source/drain regions being raised and consisting of layers of Si_xGe_{1-x} and Si_yGe_{1-y} with different band gaps and values of x and y and capable of generating carriers through impact ionization.

Pham et al. teach (e.g. Figure 9) to form FETs as FinFETs with the gate structure wrap **24** around the body portion **20** in at least two planes and consisting of a plurality of gates (Column 2 Lines 33 to 35), the gate electrode comprising doped polysilicon or metal (Column 5 Line 66 to Column 6 Line 3), the thickness of the insulating layer being thicker on the top **22** of the body portion than on the sides, the source/drain regions **33** being raised and consisting of layers of materials **32, 34** with different band gaps (e.g. Figure 5) to obtain suitable threshold voltages for high-speed logic devices while controlling extrinsic resistance (Column 1 Lines 51 to 60). It would have been obvious to a person of ordinary skill in the art at the time of invention to form FETs as FinFETs with the gate structure wrap around the body portion in at least two planes and consisting of a plurality of gates, the gate electrode comprising doped polysilicon or metal, the thickness of the insulating layer being thicker on the top of the body portion than on the sides, the source/drain regions being raised and consisting of layers of materials with different band gaps as taught by Pham et al. in the device of Ohsawa et al. to obtain suitable threshold voltages for high-speed logic devices while controlling extrinsic resistance.

Kencke et al. teach (e.g. Figure 2) to have source/drain regions **12/14** consisting of layers of Si_xGe_{1-x} and Si_yGe_{1-y} **24,26** with different band gaps and values of x and y and capable of generating carriers through impact ionization (Column 2 Lines 45 to 61) to provide better device characteristics (Column 4 Lines 1 to 5). It would have been obvious to a person of ordinary skill in the art at the time of invention to have source/drain regions consisting of layers of Si_xGe_{1-x} and Si_yGe_{1-y} with different band gaps and values of x and y and capable of generating carriers through impact ionization as taught by Kencke et al. in the device of Ohsawa et al. to provide better device characteristics.

Since the Applicant has not established the criticality of the doses stated and since these doses are in common use in similar devices in the art, it would have been obvious to one of ordinary skill in the art to use these values in the device of Ohsawa et al., Pham et al. and Kencke et al. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).*

3. Claims 8 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al., Pham et al. and Kencke et al., as applied to Claim 1 above, and further in view of Hu et al. (U.S. Patent No. 5,448,513).

Ohsawa et al., Pham et al. and Kencke et al. show most aspects of the instant invention (Paragraph 2) except for the heavily doped region of a second conductivity adjacent to one of the source/drain regions and separated form the other source/drain region. Hu et al. teach (Figure 1A) to have a heavily doped region **16** of a second conductivity adjacent to one of the source/drain regions **12** and separated form the other source/drain region **14** to use less voltage during write operations (Column 4 Lines 50 to 53). It would have been obvious to a person of ordinary skill in the art at the time of invention to have a heavily doped region of a second conductivity adjacent to one of the source/drain regions and separated from the other source/drain region as taught by Hu et al. in the device of Ohsawa et al., Pham et al. and Kencke et al. to use less voltage during write operations.

4. Claims 14 to 16, 38 to 40 and 59 to 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al., Pham et al. and Kencke et al., as applied to Claim 1 above, and further in view of Matsumoto et al. (U.S. Patent No. 6,806,537).

Ohsawa et al., Pham et al. and Kencke et al. show most aspects of the instant invention (Paragraph 2) except for the source/drain regions having a silicide in contact therewith, the silicide different for the source/drain regions. Matsumoto et al. teach (Figure 25) to silicide **45** contacts to source/drain regions **10** to reduce the gain of any parasitic bipolar transistors (Column 17 Lines 56 to 60). It would have been obvious to a person of ordinary skill in the art at the time of invention to silicide contacts to source/drain regions as taught by Hu et al. in the device of Ohsawa et al., Pham et al. and Kencke et al. to reduce the gain of any parasitic bipolar transistors.

In reference to the silicide and concentrations of the sources/drain regions, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the silicide contacts and dopant concentrations different, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

5. Claims 15 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al., Pham et al. and Kencke et al., as applied to Claim 1 above, and further in view of Takasu (U.S. Patent No. 5,307,305).

Ohsawa et al., Pham et al. and Kencke et al. show most aspects of the instant invention (Paragraph 2) except for the insulating material having a high dielectric constant. Takasu teaches (Figure 1) to use insulating material **15** having a high dielectric constant to obtain good FET characteristics (Column 17 Lines 56 to 60). It would have been obvious to a person of ordinary skill in the art at the time of invention to use insulating material having a high dielectric constant as taught by Takasu in the device of Ohsawa et al., Pham et al. and Kencke et al. to obtain good FET characteristics.

6. Claims 9, 10, 27, 36, 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa et al., Pham et al. and Kencke et al., as applied to Claim 1 above, and further in view of Yu et al. (U.S. Patent No. 6,221,724).

Ohsawa et al., Pham et al. and Kencke et al. show most aspects of the instant invention (Paragraph 2) except for the body portion containing an inert dopant. Yu et al. teach (Figure 1) to use an inert dopant **46** in a body portion **12** to suppress punch-through (Column 2 Lines 1 and 2). It would have been obvious to a person of ordinary skill in the art at the time of invention to use an inert dopant in a body portion as taught by Yu et al. in the device of Ohsawa et al., Pham et al. and Kencke et al. to suppress punch-through.

Since the Applicant has not established the criticality of the doses stated and since these doses are in common use in similar devices in the art, it would have been obvious to one of ordinary skill in the art to use these values in the device of Ohsawa et al., Pham et al. and Kencke et al. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).*

(10) Response to Argument

The Examiner will address the Appellant's first two arguments (Pages 13 to 15 of Appeal Brief): a) there is no disclosure, teaching or suggestion in the references themselves to combine these teachings, and the Final Rejection does not rely on any other explicit or implicit evidence of motivation to combine; b) Pham explicitly teaches away from using the disclosed FinFET as a storage transistor, and therefore cannot serve to create a prima facie case of obviousness.

> *a) There is no disclosure, teaching or suggestion in the references themselves to combine these teachings, and the Final Rejection does not rely on any other explicit or implicit evidence of motivation to combine*

The Appellant's argument that Pham et al. disclose is no motivation to use the disclosed FINFET as a storage transistor is a misrepresentation of the prior art as used in the Examiner's rejection of the pending claims. In particular, the Appellant repeatedly invokes unclaimed limitations "channel doping" and "carrier mobility" as evidence that Pham et al. does not teach the use of the FINFET as a storage transistor. First, "channel doping" does not appear as a limitation in any of the pending claims and, therefore, should not be considered as a basis of establishing the legitimacy of combining the prior art. Even if "channel doping" is considered, Pham does not say the channel cannot be doped. The material of the substrate, for example, used to form the fin could be doped material producing a doped channel. Intense doping is designated in the art with a "+" such as "p+" or "n+." The MOSFET of Ohsawa et al. shows a "p" doped channel (see Figure 3) not a "p+."

Although Pham et al. do not directly discuss memory applications of their invention, they do state that their invention is not limited by the embodiments presented in their specification (Column 8 Line 65 to Column 9 Line14):

> "...Although the invention has been described and illustrated with reference to specific embodiments, it is not intended that the .invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, the invention is not limited to the particular size or dimensions illustrated. In addition, the invention is not limited to any particular type of integrated circuit described herein. Furthermore, a polysilicon FinFET formed according to the teachings of the present invention may undergo or become part of a different or more complex fabrication process, provided, however, that the essential characteristics of the present invention exist in the process. Therefore, it is intended that this invention encompass all such modifications and variations which fall within the scope of the appended claims."

The motivation to use the FinFET is as stated in the Final Rejection above: "to obtain suitable threshold voltages for high-speed logic devices while controlling extrinsic resistance."

b) Pham explicitly teaches away from using the disclosed FinFET as a storage transistor, and therefore cannot serve to create a prima facie case of obviousness.

The Appellant states Pham et al. explicitly teaches away from using the FinFET as a storage transistor without explicitly pointing out the language in Pham et al. that teaches this prohibition. The Appellant discussion of "channel doping" in Pham et al. and the floating body cell in Ohsawa et al. is not evidence of "teaching away" form using the device of Pham et al. as a memory transistor. "Channel doping" does not appear as a limitation in any of the pending claims and, therefore, should not be considered as a basis of establishing the legitimacy of the rejection of the pending claims from the combination of the prior art. The evidence, as presented by the Appellant, of the inoperability of the device of combination of the prior art is not supported by the prior art. This intense doping (i.e. p+ or n+) is not present or required in the partially depleted device of Ohsawa et al. There is no explicit statement in Pham et al. that the channel is required to be undoped. The use of doped material from which the FinFET's channel is made is also not explicitly excluded. Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. *In re Susi, 440 F.2d 442, 169 USPQ 423 (CCPA 1971).* "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." *In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994).*

As correctly stated by the Appellant in the Appeal Brief, it is the gate structure wrapped around the body portion in at least two planes that is claimed by the instant invention and not a FinFET explicitly. The Examiner, in the rejection above, correctly states that the FinFET of Pham et al. has these features and that one of ordinary skill would be motivated to use this gate structure for the reasons stated.

3. Kencke does not cure the deficiencies of Pham and Ohsawa

The Appellant states that there is no motivation to combine Kencke with Pham et al. and Ohsawa and that the motivation of the criticality arguments is on the PTO to prove. As stated in the rejection above, the motivation to combine Kencke's source/drain regions consisting of layers of Si_xGe_{1-x} and Si_yGe_{1-y} with different band gaps and values of x and y and capable of generating carriers through impact ionization is to provide better device characteristics. As far as the criticality arguments, the claim language states that the dose is "approximately" between a range thus establishing the non-critically of the claimed values.

B. Claims 8 and 35 are patentable over Ohsawa, Pham, Kencke, and Hu (Ground Of Rejection B)

The Appellant sate that there is no motivation to combine Hu with Ohsawa in view of Pham and Kencke since the there already exist a word line and Ohsawa already reject a published paper by Hu et al. with a similar title and date as the patent. However, Hu et al. teach to have a heavily doped region of a second conductivity adjacent to one of the source/drain regions and separated from the other source/drain region so as to use less voltage during write operations. In reference to the article of Hu et al. as mentioned in Ohsawa et al., only what is described in the Hu et al. patent is of relevance to the rejection since the rejection is based only on that patent and not any published material by the same inventor/author.

C. – E. Grounds of rejection involving Matsumoto, Takasu and Yu

The Appellant's arguments involving these references are based upon the prior rejections involving Ohsawa, Pham and Kencke. Since the Examiner has established the validity of use of the prior art in rejection the pending claims, the rejections involving Matsumoto, Takasu and Yu are valid and should be affirmed for those reasons stated above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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